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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/238,262	01/27/99	SCHAEFER J	10191/955

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EXAMINER	
ALANKO, A	
ART UNIT	**PAPER NUMBER**
1746	5

DATE MAILED: 08/16/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No.	Applicant(s)	
	09/238,262	SCHAEFER ET AL.	
	Examiner	Art Unit	
	Anita K Alanko	1746	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☒ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 5 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. It is not clear how an "integrated circuit photoresist technique" is different or further limits a "photoresist technique."

Claim Rejections - 35 USC § 112

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "thin" is a relative term with no basis for comparison, thus rendering the claim unclear in meaning and scope. It may be simply deleted.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who

has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by O-Neill (U.S. Patent No. 5131978).

O-Neill discloses a method comprising the steps of:

- providing a wafer 10 having a surface and edge areas (Fig.3A);
- dividing the surface of the wafer into positive areas 20, to be subsequently etched in a wet chemical etching process, and negative areas including the edge areas of the wafer;
- providing the negative areas with a passivation layer 30, 32 to protect the negative areas from the subsequent wet chemical etching process (Fig.3A);
- etching the wafer in the wet chemical etching process (Fig.3D, col.5, line 53); and
- removing the passivation layer (Fig.3F, col.6, lines 25-27).

As to claims 2-4, O'Neill discloses to divide the wafer into positive and negative areas by:

- applying a nitride layer 30 (col.5, line 5); and
- structuring the nitride layer 18 using a photoresist technique (col.5, line 11) so that the positive areas are defined by a part of the surface covered with the nitride layer;
- removing the nitride layer at least in subareas of the positive areas (where channel 20 is to be etched), after the negative areas are provided and before the wafer is etched (Fig.3B);
- applying a further passivation layer 38 (col.5, lines 26-28) in the subareas, after the removal of the nitride layer 30 in the subareas and before the wafer is etched; and
- completely removing the nitride layer (Fig.3F).

As to claim 5, the photoresist technique of O'Neill is an integrated circuit photoresist technique.

As to claims 6-7, the photoresist is inherently also removed at the edge since it is eventually completely removed from the substrate after exposure and development.

As to claim 8, O'Neill discloses that the passivation layer comprises an oxide layer 32 (col.4, line 59).

5. Claims 1-3, 5-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Burns et al (U.S. Patent No. 5738757).

Burns discloses a method comprising the steps of:

- providing a wafer 10 having a surface and edge areas (Fig.1A);
- dividing the surface of the wafer into positive areas, to be subsequently etched in a wet chemical etching process, and negative areas including the edge areas of the wafer;
- providing the negative areas with a passivation layer 10, 14, 16, 18 to protect the negative areas from the subsequent wet chemical etching process (Fig.1A);
- etching the wafer in the wet chemical etching process (Fig.1E-1I, col.5, lines 6-8); and
- removing the passivation layer (Fig.1J).

The edge areas are shown as the peripheral areas in Fig.1A.

As to claim 2, Burns discloses to provide a nitride layer 14, 18 and to structure the nitride layer using a photoresist technique so that the positive areas are defined by a part of the surface covered with the nitride layer (col.5, lines 32-44).

As to claim 3, Burns discloses to remove the nitride layer in subareas (Fig.1H, col.5, lines 66-67) before the wafer is etched (Fig.1I, col.6, lines 2-10).

As to claim 5, the photoresist technique of Burns is an integrated circuit photoresist technique.

As to claims 6-7, the photoresist is inherently also removed at the edge since it is eventually completely removed from the substrate after exposure and development.

As to claim 8, Burns discloses that the passivation layer comprises an oxide layer 12 (col.5, lines 24-25).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al (U.S. Patent No. 5738757).

The discussion of Burns from above is repeated here. As to claim 9, Burns discloses that the oxide layer is grown on the wafer (col.5, lines 24-25), but does not disclose that a LOCOS process is used. Examiner takes official notice that it is conventional in the art to grow oxide layers by a LOCOS process. It would have been obvious to one with ordinary skill in the art to use a LOCOS process to form the oxide layer in the method of Burns because it is a conventional technique for forming oxide layers.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited art shows methods of etching and passivation. Zias et al shows sequential etching and masking steps (Fig.3a-3e). Yahalom shows forming an oxide on all surfaces of a wafer (Fig.1b).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anita K Alanko whose telephone number is 703-305-7708. The examiner can normally be reached on Monday-Thursday, 9:30-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Randy Gulakowski can be reached on 703-308-4333. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-7719 for regular communications and 703-305-3599 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Anita Alanko
Patent Examiner
Art Unit 1746

AKA
August 14, 2000